San José State University
Department of Computer Science

CS 147 Computer Architecture

Instructor: Soon Tee Teoh
Email: *soontee.teoh@sjsu.edu*
Office Hours: By appointment only. I am typically available Mon/Wed/Fri 5 pm till midnight. Email me 24 hours in advance to schedule a meeting.
Office Location: https://sjsu.zoom.us/j/132407857

Class Days/Time: Tue/Thu 4:30 - 5:45 pm
Classroom: https://sjsu.zoom.us/j/132407857
Prerequisites: CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Format
This course will be taught primarily via classroom presentations. Zoom lectures will be recorded and posted on the “Pages” tab on Canvas. Students are expected to be present during the scheduled exams during the class period.

Canvas Course Website
Course materials, syllabus, assignments, grading criteria, exams, and other information will be posted on the Canvas Learning Management System course login website at http://sjsu.instructure.com.
You are responsible for regularly checking these websites to learn of any updates. You can find Canvas video tutorials and documentations at http://ges.sjsu.edu/canvas-students.

Course Catalog Description
Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLO)
Upon successful completion of this course, you will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes

- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware designs

BS in Computer Science Program Outcomes Supported

These are the BSCS Program Outcomes supported by this course.

- An ability to apply knowledge of computing and mathematics to solve problems
- An ability to analyze a problem, to identify and define the computing requirements appropriate to its solution
- An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs
- An ability to use current techniques, skills, and tools necessary for computing practice
- An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices

Academic Integrity

You may study together and discuss the assignments, but what you turn in must be your individual work. Copying code from another student's program or sharing your program code are equally serious violations of academic integrity. Never use code you find on the web, unless you have the instructor's permission, and then you must give proper attribution in your comments. This is similar to giving attribution to a quote that you use in a term paper. Assignment submissions will be checked for plagiarism using Moss from the Department of Computer Science at Stanford University. See http://theory.stanford.edu/~aiken/moss/.
Violators of academic integrity will suffer severe sanctions, including academic probation. Students who are on academic probation are not eligible for work as instructional assistants in the university or for internships at local companies.

Recommended Texts

LOGIC & COMPUTER DESIGN FUNDAMENTALS Author: MANO & KIME ISBN: 9780131989269 Publication Date: 06/15/2007 Publisher: PEARSON

COMPUTER ORGANIZATION and DESIGN | Edition: 5 Author: DAVID A. PATTERSON
ISBN:9780124077263 Publication Date:10/10/2013 Publisher:ELSEVIER

Software to Install
Later in the semester, we will be using VHDL. At that time, you will need to install a VHDL simulator, such as GHDL, on your computer. To view the output, you will also need to install a viewer such as GTKWave.

Course requirements and assignments
There will be homework assignments and exams.

Assignments
There will be multiple homework assignments throughout the semester. Each assignment will be worth a specified maximum number of points. Assignments can be turned in within 48 hours late for 20% deduction. After 48 hours, no submission is allowed (it will get a 0 score).

Exams
All exams are open-book. You can refer to all class material. However, you may not communicate with any other person, or search solutions on the Internet. The exams will test understanding (not memorization) of the material taught during the semester. Instant messaging, e-mails, texting, tweeting, file sharing, or any other forms of communication with anyone else during the exams will be strictly forbidden. There can be no make-up exams unless there is a documented medical emergency.

The university's syllabus policies
- University Syllabus Policy S16-9 at http://www.sjsu.edu/senate/docs/S16-9.pdf
- Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

"Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally 3 hours per unit per week with 1 of the hours used for lecture) for instruction or preparation/studying or course related activities including but not limited to internships, labs, clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus."

Grading Information
Your final class grade will be weighted as follows:
Homework Assignments: 40%
3 Exams: 60% (15%, 15% and 30% respectively)

Final score to letter grade conversion is as follows:

Overall Score	Grade
100 - 96	A
95.99 - 92	A-
91.99 - 88	B+

87.99 - 84	B
83.99 - 80	B-
79.99 - 77	C+
76.99 - 74	C
73.99 - 70	C-
69.99 - 0	F

Classroom Protocol

It is very important for each student to attend classes and to participate. Cell phones in silent mode, please. No use of electronic devices (phones, tablets, laptop computers etc.) in class, except to take notes.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/.

Course Schedule

Week	Tue	Thu
0		1/27/2022
		Introduction
1	2/1/2022	2/3/2022
	Logic Gates, Delay	Karnaugh Maps
2	2/8/2022	2/10/2022
	Decoders, Multiplexers	Adders, Numbers
3	2/15/2022	2/17/2022
	Sequential Circuits	State Diagrams
4	2/22/2022	2/24/2022
	Registers	Datapath
5	3/1/2022	3/3/2022

	Review	Exam 1
6	3/8/2022	3/10/2022
	ALU, Shifter	Control Word
7	3/15/2022	3/17/2022
	Control Word	Instruction Set Architecture
8	3/22/2022	3/24/2022
	VHDL, Control	Floating Point, Pipeline
9	3/29/2022	3/31/2022
	Spring Break	Spring Break
10	4/5/2022	4/7/2022
	Homework demo	RISC
11	4/12/2022	4/14/2022
	Hazards	CISC, Parallelism
12	4/19/2022	4/21/2022
	Review	Exam 2
13	4/26/2022	4/28/2022
	Memory and Caches	Cache Replacement Policies
14	5/3/2022	5/5/2022
	Virtual Memory	Multiplication, I/O
15	5/10/2022	5/12/2022
	Review	Exam 3