San José State University
Electrical Engineering Department
EE 182 Section 1 - Analog and Mixed-Signal IC Test Development
Fall 2021

Course and Contact Information
Instructor(s): JeongHee(John) Kim
Office Location: Engineering Building, Room 259
Telephone: (408) 924-3950
Email: jeonghee.kim@sjsu.edu or jeonghee_kim@yahoo.com
Office Hours: Thursday 16:00-17:40 online
Class Days/Time: Mo, We 16:00-17:15
Classroom: Engineering Building 343
Prerequisites: EE112, EE118, EE 122 with grades of C- or above. EE102 can be taken concurrently

Course Description
Introduction to analog and mixed-signal IC and component measurements and automated testing. Test specifications, methods, techniques, and interfaces. Measurement accuracy, correction, and calibration. Automated test equipment (ATE) hardware and software. DAC/ADC testing and DSP-based testing. Analog and mixed-signal design for test (DFT). Laboratory exercises and mini projects.

Faculty Web Page and MYSJSU Messaging
Course materials such as syllabus, handouts, notes, assignment instructions, etc. are all on class Canvas at http://sjsu.instructure.com. You are responsible for regularly checking class message broadcasted from Canvas and/or sent to your email address on MySJSU account to learn of any updates.

Course Goals and Student Learning Outcomes (CLO)
Upon successful completion of this course, students will be able to:

1. Understand analog, digital, mixed-signal technologies and CMOS fabrication processes.
2. Understand characterization versus production testing.
3. Understand industry practices and testing environment as well as best practices in test methods and techniques.
4. Perform basic DC measurements on components and integrated circuits.
5. Apply techniques of calibration and correction to achieve a given measurement accuracy.
6. Test design, measure, and analyze collected test data.
7. Understand the advantages of DSP-based testing.
8. Explain the issues involved in test economics and motivation for Design for Test (DFT).

The above Course Learning Outcomes satisfy the following ABET Student Outcomes (SO).
SO2: An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.

SO4: An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.

SO6: An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

**Required Texts/Readings**

**Textbook**

**Other Readings**
1. Instructor’s notes and industry data sheets and equipment manuals on class Canvas
2. Laboratory manual on class Canvas
3. AtvanTest Web (https://www.advantest.com/)

**Other Technology Requirements/Equipment/Material**
The Student Version of Matlab, C++, Python, or Octave (free and similar to Matlab)) is recommended for supporting numerical computations when needed. It’s available from the Mathworks Inc. (http://www.mathworks.com/academia/student_version/). Matlab and many of its “toolboxes” are available on the EE Department PC’s in room ENG387 (an open lab; open times are posted on the door). Matlab may be used to demonstrate some topics in the class.

**Course Requirements and Assignments**

**Lectures**
The course will follow the selected subjects as listed on the course description. Additional theory and examples will be given and discussed in class as much as time permits.

- Please note that lecture and lab materials are NOT solely based on the required text and so students are responsible for following up the lecture in order to prepare themselves for the exams
- Students are responsible for the reading the text, handouts, lecture presentations in the classroom board, etc.
- Students are responsible for following up and keeping track of the in-class lecture materials.
- Students are responsible for finding and reading additional books, papers, examples, etc. in order to gain more understanding of the materials discussed in the lectures.

**Midterm and Final Exams and Design Project**
There will be **one midterm exam, final exam, labs, hws and quizzes**. The Final exam date is posted by the university. Since make-up exams will NOT be allowed, please make sure that you are able to
attend all exams at the indicated scheduled dates and times (from the beginning of the semester) in order to register for the course.

☐ All exams are closed-book exams.
  • One sheet (double-side 8.5x11) of hand-written notes is allowed for each midterm exam and two sheets of hand-written notes are allowed for the final exam.
  • Only basic calculators are allowed.

☐ There will be no make-up exams

Homework Assignments
• Lab & Homework assignments and/or lab exercises will be given with due dates
  • If you turn in assignments and labs late, maximum of 10% credits will be given.
  • Each lab report has to follow directions given in the class.

• If unreasonable or out of common sense behavior happens in the class, one will be asked to leave from the class and will be given “F” grade. (No feet on a table or chair, taking hat off, no cellphone use or web surfing, no talking with neighbors). And I will drop you from the class if the class is disturbed unreasonably with my right.

• No food is allowed (Water is ok). All the exams and quizzes are done in the class and only allowed to use pencil, eraser (no pen) and calculator.

• Lab report and Homework must be submitted in class on time.

• Do NOT submit HW via email.

• Late submission will NOT be accepted (absolutely!).

• There is no make-up labs and homework

“Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practice. Other course structures will have equivalent workload expectations as described in the syllabus.”

Final Examination or Evaluation
• The final exam is an in-class exam.
• The exam date and time is defined in Course Schedule (last page of this syllabus) or can be found in the university final exam schedule.
• It is a comprehensive exam; the exam covers the all materials covered in the class throughout the semester.

The assignments for this course include:
• Seven (7) laboratory exercises with homework questions and reports
• One (1) midterm exam
• One (1) final exam
• HW & Quiz

Final Examination or Evaluation

Final examination date and time is scheduled by the university. The exam will be comprehensive exam such that topics of the whole course can be covered in the exam.

Grading Information

The overall course grades (letter-grades) will be assigned based on a defined grading standard as shown below. The weights of the whole course work assignments are:

1. Homework assignments, Projects & Quizzes 15% (Quiz=HW)
2. One midterm exam 15%
3. Final exam 15%
3. Labs 55%

And the overall course grade (letter-grade) will be assigned based on the distribution below:

Grading criteria (Example: 74% results in a grade of C+):


University Policies

Per University Policy S16-9 (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on Syllabus Information web page (https://www.sjsu.edu/curriculum/courses/syllabus-info.php). Make sure to visit this page to review and be aware of these university policies and resources.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”
**Measures Dealing with Occurrences of Cheating**

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student’s second offense in any course will result in a Department recommendation of suspension from the University.

**EE 182-01 - Analog and Mixed-Signal IC Test Development**
**Fall 2021 Course Schedule**  (tentative)

*Schedule is subject to change with fair notice by email and on class Canvas*
<table>
<thead>
<tr>
<th>Weeks</th>
<th>Lab</th>
<th>Tools Used</th>
<th>Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>1. Programming</td>
<td>Python IDE, Octave, C++ (Does not require visiting Advantest office)</td>
<td>Introduction to the typical programming tasks in the job environment. No need to visit Advantest.</td>
</tr>
<tr>
<td>3-4</td>
<td>2. V93000 SmarTest 7 Tester Start-up and Tools Used in Subsequent Labs</td>
<td>V93K Test System SmarTest 7.5.4</td>
<td>Familiarize new users in launching V93000 SmarTest 7 and the tools required in subsequent labs. Also, introduce users to typical digital and DC instruments needed to test mixed signal devices</td>
</tr>
<tr>
<td>5-6</td>
<td>3. R, C, and L Testing</td>
<td>V93K Test System SmarTest 7.5.4 and SJSU Custom Loadboard</td>
<td>To study, test and understand the effects and importance of discrete components (Resistors, Capacitors, and Inductors)</td>
</tr>
<tr>
<td>7</td>
<td>4. DIB (Device Interface Board) Overview and Design Considerations</td>
<td>None required. (Does not require visiting Advantest office)</td>
<td>Introduces the major DIB design parameters that should be considered when designing DIB’s as well as the other hardware used to dock DIB’s to the test system Test Head</td>
</tr>
<tr>
<td>8-9</td>
<td>5. ADC</td>
<td>V93K Test System SmarTest 7.5.4 and SJSU Custom Loadboard</td>
<td>The objective is to explore ADC testing using the V93000 ATE and the SJSU Custom Daughter Board</td>
</tr>
<tr>
<td>10-11</td>
<td>6. DAC</td>
<td>V93K Test System SmarTest 7.5.4 and SJSU Custom Loadboard</td>
<td>The objective is to explore DAC testing using the V93000 ATE and the SJSU Custom Daughter Board</td>
</tr>
<tr>
<td>12-13</td>
<td>7. RC Filter</td>
<td>V93K Test System SmarTest 7.5.4 and SJSU Custom Loadboard</td>
<td>To study, test and understand the effect and importance of RC filter circuits</td>
</tr>
<tr>
<td>13-14</td>
<td>8. Mini-project: DAC MTPR</td>
<td>V93K Test System SmarTest 7.5.4 and SJSU Custom Loadboard</td>
<td>Final project based on Renesas “Missing Tone Power Ratio” (MTPR) DAC test spec</td>
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<td>15</td>
<td>Final Exam:</td>
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