HIU YUNG WONG

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Education

- **UNIVERSITY OF CALIFORNIA, BERKELEY (UCB)**
  Ph.D.: Electrical Engineering and Computer Science — July 2006
  Thesis: ***Advanced Gate Processes for Nanoscale CMOS***
  Advisor: Prof. Tsu-Jae King Liu
  Major: *Electronic Device Physics and Processing*
  Minor: *Integrated Circuits* (Internal), *Quantum Mechanics* (External)

- **THE CHINESE UNIVERSITY OF HONG KONG (CUHK)**
  M. Phil.: Computer Science and Engineering — July 2001
  Thesis: ***Matching Properties and Applications of Compatible Lateral Bipolar Transistors***
  Advisor: Prof. Philip Heng Wai Leong

  B.Eng. (First class honor): Computer Engineering — July 1999
  Minor: Business Administration
  Thesis: ***Solving Constraint Satisfactory Problems using FPGAs***
  Advisor: Prof. Philip Heng Wai Leong

Professional Experience

Visiting Scholar, TCAD Simulation, Prof. King-Liu's group — **UC Berkeley** — **2019-2020**

Assistant Professor, Electrical Engineering — **San Jose State University** — **2018-**

- Machine Learning to Discover Physical Models and Process/Circuit Debugging
- Memory material characterization and simulation for leakage
- Compact Model for Neuromorphic Simulation
- Calibration and Simulation of Novel WBG Power Device for Electric Vehicles and others
- Electrically Variable Gate Length Transistor for sub-5nm nodes
- Cryogenic Calibration of CMOS Devices for Quantum Computing Interface
- Reliability Modeling of IoT Devices

Senior Staff Applications Engineer — **Synopsys Inc.** — **2009 – 2018**

- **Reliability simulations on GaN defects and FinFET/nanowire NBTI**
- **Novel power device and reliability simulations/modeling (GaN, Ga2O3, Diamond)**
- **Expert/Champion on the following simulation tools**
  - SDevice, SProcess, SBand/Sub-band BTE, Monte Carlo Transport, NEGF, STT-RAM, ReRAM, Ab-initio to TCAD link
- **Strong relationship with customers and understanding of the state of the art technologies**
- **Technical know-how**
  - Delivered more than 20 technically successful TCAD simulation benchmarks on our customers' products including Si LDMOS, GaN devices, SiC IGBT, Avalanche Photo Diodes (APD), opto-electronics, ReRAM, HCI effects in SOI
- **Pioneer Machine Learning** in TCAD simulations and applications

MTS Integration Engineer — **Spansion (AMD/Fujitsu) Inc.** — **2006 – 2009**

- 45nm/32nm NOR Flash Memory Technology Process Integration and Development
- Designed and verified 45nm Test Chip test structures layout
- STI, bitline, poly gate and CoSi modules optimization and Si defect studies

- Periphery devices development and integration including simulation and bench measurements

Internship **Cypress Semiconductor** **2004 – 2005**

- Designed and applied non-melt and melt excimer laser annealing experiments to 200mm integration lots to mitigate poly gate depletion
- Owned 200mm integration with various novel gate and source/drain engineering splits

6'' CMOS baseline Process Development Team Member **UCB Microfabrication Lab** **2002-2005**

- Performed full CMOS process flow and device simulations
- Performed bench characterizations: IV, CV, Oxide BV, mobility extraction, ring oscillator measurement

Services

College Assessment Committee, College of Engineering, 2018-
Chair Review Committee, Electrical Engineering, 2021
Associate Dean Search Committee, College of Engineering, 2021
Department Graduate Curriculum Committee, Electrical Engineering, 2019-
Department Assessment Committee, Electrical Engineering, 2019-
Contributor, Strategic Plan, College of Engineering, 2019

Professional Activities

Editor:

- Associate Editor, IEEE Access (2020 -)
- Guest Editor, Micromachines, special issue on "Novel Ultra Wide Bandgap Power Devices and Materials", 2020
- Guest Editor, Journal of Vacuum Science and Technology B, special issue on "Reliability and Stress-related Phenomena in Nano and Microelectronics", 2020

Conference Organizer:

- Technical Program Committee (TPC), International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) (2020-)
- Vice Chair, 16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics (IRSP19)
- Member of International Program Committees for The IASTED International Conference on Control and Optimization of Renewable Energy Systems CORES 2019
- Workshop Moderator, "Circuit Reliability: Advanced nodes concerns and CAD tools flows" 2018 IEEE International Reliability Physics Symposium (IRPS)

Senior Member of Institute of Electrical and Electronics Engineers (IEEE)

IEEE EDS-SCV/SF Chapter Officer

- Treasurer (2019-)
- Secretary (2018-2019)
- Executive committee board (2018-)

Reviewer:
Grants/Awards: 2019 NASA Fellowship (Program Officer, Brenda Collins)

Journals: IEEE Electron Device Letters (EDL), Applied Physics Letters (APL), IEEE Journal of Electron Devices Society (J-EDS), IEEE Access, IEEE Transaction on Electron Devices (TED), IEEE Transaction on Nanotechnology (TNANO), Applied Physics Letters (APL), Diamond & Related Materials, IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), IET Circuits, Devices & Systems, Journal of the Electrochemical Society, Electrochemical and Solid-State Letters, Solid-State Electronics, book reviewer for Bentham Science Publishers.

Outreach:

- Judge**:** The Synopsys Championship (the Santa Clara County science fair for students in grades 6-12), Sciencepalooza! (for students in grades 9-12 in East San José)
- Summer Class: "Introduction to Python Programming and Machine Learning" 6/30/2020-7/1/2020 for Downtown College Prep high school students.

Grants

Awarded (US$ 973K since Fall 2018):

Extramural:

G1. **National Science Foundation**, CAREER: Understanding and Modeling of Cryogenic Semiconductor Device Physics down to 4.2K, US$500K, PI (100%) (2021-2026)
G2. **Applied Materials Inc,** Power Device Simulation and Optimization, US$65K, PI (100%) (2021)
G3. **Synopsys Inc,** Materials Modeling Research Project, US$15K, PI (100%) (2020-2021)
G4. **Atomera Inc,** Modeling and Simulation of MST, US$75K, PI (100%) (2020)
G5. **Department of Energy, PowerAmerica,** Development of Low-Cost Graduate Course with Virtual Fab and Hands-on Circuit Lab Experience to Prepare Students to Work in the SiC Industry in Silicon Valley, US$50K, PI (50%) (2019-2020)
G6. **NASA,** Chip Design for Self-Healing Electronics, US$ 50K, PI (100%) (2019-2020)
G7. **Department of Defense, Naval Surface Warfare Center Crane Division**, Radiation Hardness Projection and Optimization of sub-10nm Technology Node SRAM through Design-Technology-Co-Optimization (DTCO) Simulations, US$ 26K, PI (100%) (2019)
G8. **Atomera Inc,** Modeling and Simulation of MST, US$27.5K, PI (100%) (2019)
G9. **Synopsys Inc,** Materials Modeling Research Project, US$30K, PI (100%) (2019-2020)
G10. **Atomera Inc,** CMOS applications of MST film using TCAD, US$25K, sole PI (100%) (2019)

Internal (SJSU):

G11. **SJSU, The Level-Up Grant,** Development of Cryogenic Transistor Model for Quantum Computing Peripherals, US$9,350, PI (100%) (2020-2021)
G12. **SJSU COE,** Design Technology Co-Optimization (DTCO) Framework for Neuromorphic Computing: from Device to System, US $100,000, PI (34%) (2019-2020)

Patents

P1. **Hiu Yung Wong** and Rimvydas Mickevicius. Threading dislocation in GaN (or other materials) is used to generate Physical Unclonable Function for GaN IoT (or other materials or non-IoT applications) US Provisional Patent App. 62/712,259, 2018. (Non-Provisional filed)

P2. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Machine Learning for Optimizing Setups for Accurate, Speedy and Robust TCAD Simulations. US Provisional Patent App. 62/581,068. Filed 2017. (Non-Provisional filed)

P3. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Constricted Junction-less FinFET/ Nanowire/ Nanosheet with normally-off VTH, high ION and low leakage. U.S. Patent No. 10,777,638. Issued September 15, 2020.

P4. **Hiu Yung Wong** and Rimvydas Mickevicius. A new local Band-to-Band Tunneling (BTBT) model for more accurate and speedy TCAD simulations. U.S. Patent No. 10,769,339. Issued September 8, 2020.

P5. **Hiu Yung Wong**, Victor Moroz and Qiang Lu. Anti-punch-through implant or its extension/variations as heater for on-chip self-heating and self-annealing. U.S. Patent No. 10,699,914. Issued June 30, 2020.

P6. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Normally-off Gallium Oxide Field-Effect Transistor. U.S. Patent No. 10,644,107. Issued May 5, 2020.

P7. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Monolithically Integrated III-Nitride Cascode Circuit for High Voltage Application. U.S. Patent No. 10,403,625. Issued September 3, 2019.

P8. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Heterojunction Field Effect Transistor Device with Serially Connected Enhancement Mode and Depletion Mode Gate Regions. U.S. Patent No. 10,128,232. Issued November 13, 2018.

P9. **Hiu Yung Wong**, Nelson de Almeida Braga and Rimvydas Mickevicius. Tined gate to control threshold voltage in a device formed of materials having piezoelectric properties. U.S. Patent No. 9,837,523. filed 13 Apr 2016 and issued 5 Dec 2017.

P10. Eunha Kim, Wen Yu, Minh-Van Ngo, Kyunghoon Min and **Hiu Yung Wong**. Forming metal-semiconductor films having different thicknesses within different regions of an electronic device. US Patent 7,880,221, filed 19 Dec 2008, and issued 1 Feb 2011.

P11. Eunha Kim, Wen Yu, Minh-Van Ngo, Kyunghoon Min and **Hiu Yung Wong**. Forming metal-semiconductor films having different thicknesses within different regions of an electronic device. US Patent 7,482,217, filed 3 Dec 2007, and issued 27 Jan 2009.

Awards

- NSF CAREER Award, 2021
- The 2021 Newnan Brothers Award for Faculty Excellence, demonstrate excellence in some combination of teaching, service to students, and/or research.
- San Jose State University Grants Academy award, 2019
- Synopsys Outstanding Contribution to Results Award (For supporting foundry FinFET simulation), 2013
- Synopsys Outstanding Contribution to Results Award (For leading power device simulation), 2010
- Synopsys Excellence Award (1 out of every ~500 employees), 2010
- Sir Edward Youde Memorial Fellowships for Overseas Studies, 2001

Book Chapter

Chatterjee, B., Shoemaker, D., **Wong, H.**, & Choi, S. Electro-thermal modeling of AlGaN/GaN HEMTs. In Anderson, Travis; Tadjer, Marko (Eds.), Elsevier. [In preparation].

Peer-Reviewed Journal Papers (+: Supervised Students)

J1. **Harsaroop Dhillon**[+]**,** Kashyap Mehta[+], Ming Xiao, Boyan Wang, Yuhao Zhang, and **Hiu Yung Wong**, "TCAD-Augmented Machine Learning with and without Domain Expertise," in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2021.3073378.

J2. **A. Elwailly**[+], J. Saltin[+], M. J. Gadlage and **H. Y. Wong**, "Radiation Hardness Study of LG = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," in IEEE Transactions on Electron Devices, vol. 68, no. 5, pp. 2289-2294, May 2021, doi: 10.1109/TED.2021.3067855.

J3. **K. Mehta**[+] and **Hiu Yung Wong**, "Prediction of FinFET Current-Voltage and Capacitance-Voltage Curves Using Machine Learning With Autoencoder," in *IEEE Electron Device Letters*, vol. 42, no. 2, pp. 136-139, Feb. 2021, doi: 10.1109/LED.2020.3045064.

J4. Fei Ding, **Hiu-Yung Wong** and Tsu-Jae King Liu, "Design optimization of Sub-5nm Node Nanosheet Field Effect Transistors to Minimize Self-Heating Effects," Journal of Vacuum Science and Technology B, B 39, 013201 (2021); https://doi.org/10.1116/6.0000675. **(Editor's Pick)**

J5. **Hiu Yung Wong**, Ming Xiao, Boyan Wang, Yan Ka Chiu[+], Xiaodong Yan, Jiahui Ma, Kohei Sasaki, Han Wang, and Yuhao Zhang, "TCAD-Machine Learning Framework for Device Variation and Operating Temperature Analysis With Experimental Demonstration," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 992-1000, 2020, doi: 10.1109/JEDS.2020.3024669.

J6. Uma Sharma, Meng Duan, Himanshu Diwakar, Karansingh Thakor, **Hiu Yung Wong**, Steve Motzny, Denis Dolgos and Souvik Mahapatra, "TCAD Framework for HCD Kinetics in Low VD Devices Spanning Full VG/VD Space," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2020.3021360..

J7. Cyril Buttaya, **Hiu-Yung Wong**, Boyan Wang, Ming Xiao, Christina DiMarino and Yuhao Zhang, "Surge Current Capability of Ultra-Wide-Bandgap Ga2O3Schottky Diodes," Microelectronics Reliability, Volume 114, November 2020, 113743. 10.1016/j.microrel.2020.113743.

J8. **K. Mehta**[+], S. S. Raju[+], M. Xiao, B. Wang, Y. Zhang and **H. Y. Wong**, "Improvement of TCAD Augmented Machine Learning Using Autoencoder for Semiconductor Variation Identification and Inverse Design," in IEEE Access, vol. 8, pp. 143519-143529, 2020, doi: 10.1109/ACCESS.2020.3014470.

J9. **J. Saltin**[+], N. C. Dao, P. H. W. Leong and **H. Y. Wong**, "Energy Filtering Effect at Source Contact on Ultra-Scaled MOSFETs," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 662-667, 2020, doi: 10.1109/JEDS.2020.2981251.

J10. **Hiu Yung Wong** and Armand Tenkeu[+], "Advanced TCAD Simulation and Calibration of Gallium Oxide Vertical Transistor," ECS Journal of Solid State Science and Technology 9 (3), 035003, 2020.

J11. **Hiu-Yung Wong**, Denis Dolgos, Lee Smith, Rimvydas V. Mickevicius, "Modified Hurkx Band-to-Band-Tunneling Model for Accurate and Robust TCAD Simulations," Microelectronics Reliability, Volume 104, January 2020, 113552.

J12. Boyan Wang, Ming Xiao, Xiaodong Yan, **Hiu Yung Wong**, Jiahui Ma, Kohei Sasaki, Han Wang, and Yuhao Zhang, "High-voltage vertical Ga2O3 power rectifiers operational at high temperatures up to 600 K", Appl. Phys. Lett. 115, 263503 (2019); https://doi.org/10.1063/1.5132818.

J13. Ravi Tiwari, Narendra Parihar, Karansingh Thakor, **Hiu Yung Wong,** Steve Motzny, Munkang Choi, Victor Moroz and Souvik Mahapatra, "A 3-D TCAD Framework for NBTI, Part-I: Implementation Details and FinFET Channel Material Impact, in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2086-2092, May 2019.

J14. Ravi Tiwari, Narendra Parihar, Karansingh Thakor, **Hiu Yung Wong,** Steve Motzny, Munkang Choi, Victor Moroz and Souvik Mahapatra, "A 3-D TCAD Framework for NBTI, Part-II: Impact of Mechanical Strain, Quantum Effects and FinFET Dimension Scaling, in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2093-2099, May 2019.

J15. **Hiu Yung Wong,** Nelson Braga and R. V. Mickevicius, "Enhancement Mode Recessed Gate and Cascode Gate Junctionless Nanowire with Low Leakage and High Drive Current," in IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 4004-4008, Sept. 2018.

J16. P. Pfäfflia, **H.Y. Wong**, X. Xu, L. Silvestria, X.W. Lin, T. Yang, R. Tiwari, S. Mahapatra, S. Motzny, V. Moroz and Terry Ma, "TCAD Modeling for Reliability," Microelectronics Reliability, Volumes 88–90, September 2018, Pages 1083-1089.

J17. **Hiu Yung Wong,** Nelson Braga and R. V. Mickevicius, "Prediction of highly scaled hydrogen-terminated diamond MISFET performance based on calibrated TCAD simulation," Diamond and Related Materials, Volume 80, November 2017, Pages 14-17.

J18. **Hiu Yung Wong**, Nelson Braga, R. V. Mickevicius, " Normally-off GaN HFET based on Layout and Stress Engineering ", IEEE Electron Device Letters, 37 (12), 1621-1624.

J19. Subrat Mishra, **Hiu Yung Wong**, Ravi Tiwari, Ankush Chaudhary, Rakesh Rao, Victor Moroz and Souvik Mahapatra, "TCAD-based NBTI Predictive Model for Sub-20nm node Device Design Considerations", IEEE Transactions on Electron Devices, 63 (12), 4624-4631.

J20. Jin-Woo Han, **Hiu-Yung Wong**, Nelson Braga, Dong-Il, Moon and Meyya Meyyappan, "Stringer Gate FinFET on Bulk Substrate", IEEE Transactions on Electron Devices, 63 (9), 3432-3438.

J21. Victor Moroz, **Hiu Yung Wong**, Munkang Choi, Nelson Braga, R. V. Mickevicius, Yuhao Zhang, Thomas Palacios, "The Impact of Defects on GaN Device Behavior: Modeling Dislocations, Traps, and Pits", ECS J. Solid State Sci. Technol. 2016, volume 5, issue 4, P3142-P3148. **(INVITED PAPER)**

J22. Yuhao Zhang, Min Sun, **Hiu-Yung Wong**, Yuxuan Lin, Puneet Srivastava, Christopher Hatem, Mohamed Azize, Daniel Piedra, Lili Yu, Takamichi Sumitomo, Nelson de Almeida Braga, Vidas Mickevicius, and Tomás Palacios, "Origin and

Control of Off-State Leakage Current in GaN-on-Si Vertical Diodes ", IEEE Transactions on Electron Devices, Vol. 62, No.7, 2155-2161, 2015.

J23. **Hiu Yung Wong**, H. Takeuchi, T-J King, M. Ameen, and A. Agarwal, "Elimination of Poly-Si Gate Depletion for Sub-65nm CMOS Technologies by Excimer Laser Annealing", IEEE Electron Device Letters, Vol. 26, No. 4, pp. 234-236, 2005.

J24. Neil N. H. Ching, **H. Y. Wong**, Wen J. Li, Philip H. W. Leong and Zhiyu Wen, "A laser-micromachined multi-modal resonating power transducer for wireless sensing systems", Sensors and Actuators A: Physical, Vol. 97-98, pp. 685-690, 2002.

J25. P. H. W. Leong, C. W. Sham, W. C. Wong, **H. Y. Wong**, W. S. Yuen and M. P. Leong, "A Bitstream Reconfigurable FPGA Implementation of the WSAT algorithm", IEEE Transactions on VLSI Systems, Vol. 9, No. 1, pp. 197-201, 2001

J26. W. J. Li, G. M. H. Chan, N. N. H. Ching, P. H. W. Leong and **H. Y. Wong**, "Dynamical Modelling and Simulation of a Laser-micromachined Vibration-based Micro Power Generator", International Journal of Nonlinear Sciences and Simulation, Vol. 1, pp. 345-353, 2000.

Peer-Reviewed Conference Papers (+: Supervised Students)

C1. **Fanus Arefaine**[+], Meng Duan, Ravi Tiwari, Lee Smith, Souvik Mahapatra, and **Hiu Yung Wong**, "Using Long Short-Term Memory (LSTM) Network to Predict Negative-Bias Temperature Instability," Accepted to IEEE 2021 International Conference on Simulation of Semiconductor Processes and Devices.

C2. **Hector Morrell**[+] and **Hiu Yung Wong**, "Study of using Quantum Computer to Solve Poisson Equation in Gate Insulators," Accepted to IEEE 2021 International Conference on Simulation of Semiconductor Processes and Devices.

C3. **Prabjot Dhillon**[+], Nguyen Cong Dao, Philip H. W. Leong, and **Hiu Yung Wong**, "TCAD Modeling of Cryogenic nMOSFET ON-State Current and Subthreshold Slope," Accepted to IEEE 2021 International Conference on Simulation of Semiconductor Processes and Devices.

C4. Daniel Connelly, **Hiu Yung Wong**, Richard Burton, Hideki Takeuchi, Robert Mears, "RFSOI n-MOSFET OI-Layer Ground-Plane Engineering with Quasi-3D Simulations," Accepted to IEEE 2021 International Conference on Simulation of Semiconductor Processes and Devices.

C5. **A. Raol**[+], T. Jiao, C. Shashidhara and **H. Y. Wong**, "Fully-Coupled Simulation of the Temperature Effect on Negative Capacitance Ferroelectric Devices," 2021 IEEE Latin America Electron Devices Conference (LAEDC), 2021, pp. 1-4, doi: 10.1109/LAEDC51812.2021.9437945.

C6. A. Shimbori, **H. Y. Wong** and A. Q. Huang, "Comprehensive Comparison of Fabricated 1.6-kV Punch-Through Design Ni/n-SiC Schottky Barrier Diode with Ar+ Implant Edge Termination and Heterojunction p-NiO/n-SiC Diode," 2021 IEEE Latin America Electron Devices Conference (LAEDC), 2021, pp. 1-4, doi: 10.1109/LAEDC51812.2021.9437747.

C7. **Johan Saltin**[+], Adam Elwailly[+], and **Hiu Yung Wong**, "FinFET and Nanowire SRAM Radiation Hardness Studies using Ab initio-TCAD Simulation Framework," **Accepted** by Government Microcircuit Applications & Critical Technology Conference (GOMAC), 2021.

C8. **H. Cao**[+], T. Lam, H. Nguyen, A. Venkattraman, D. Parent and **H. Y. Wong**, "Study of ReRAM Neuromorphic Circuit Inference Accuracy Robustness using DTCO Simulation Framework," 2021 IEEE Workshop on Microelectronics and Electron Devices (WMED), 2021, pp. 1-4, doi: 10.1109/WMED49473.2021.9425210.

C9. **Sophia Susan Raju**[+], Boyan Wang, Kashyap Mehta[+], Ming Xiao, Yuhao Zhang, and **Hiu Yung Wong**, "Application of Noise to Avoid Overfitting in TCAD Augmented Machine Learning," IEEE 2020 International Conference on Simulation of Semiconductor Processes and Devices, pp. 351-354, doi: 10.23919/SISPAD49475.2020.9241654.

C10. **Hiu Yung Wong**, "Calibrated Si Mobility and Incomplete Ionization Models with Field Dependent Ionization Energy for Cryogenic Simulations," IEEE 2020 International Conference on Simulation of Semiconductor Processes and Devices, pp193-196, doi: 10.23919/SISPAD49475.2020.9241599.

C11. **A. Nguyen**[+], H. Nguyen[+], S. Venimadhavan[+], A. Venkattraman, D. Parent and **H. Y. Wong**, "Fully Analog ReRAM Neuromorphic Circuit Optimization using DTCO Simulation Framework," 2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Kobe, Japan, 2020, pp. 201-204, doi: 10.23919/SISPAD49475.2020.9241635.

C12. **Adam Elwailly**[+], Ming Xiao, Yuhao Zhang, and **Hiu Yung Wong**, "Design Space of Vertical Ga2O3 Junctionless FinFET and its Enhancement with Gradual Channel Doping," IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia 2020, pp. 41-45.

C13. Cyril Buttaya, **Hiu-Yung Wong**, Boyan Wang, Ming Xiao, Christina DiMarino and Yuhao Zhang, "Surge Current Capability of Ultra-Wide-Bandgap Ga2O3Schottky Diodes," **Accepted** by The 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Athens, 2020.

C14. Shuntaro Fujii, Hideki Takeuchi, Soichi Morita, Tatsushi Yagi, Shohei Hamada, Toshiro Sakamoto, Shinji Kawaguchi, Naoki Ishigami, Atsushi Okamoto, Shuji Ikeda, **Hiu-Yung Wong**, Robert J. Mears and Tsutomu Miyazaki, "Analysis of the

Effects of Boron Transient Enhanced Diffusion on Threshold Voltage Mismatch in Steep Retrograde Doping NMOSFETs with Inserted Oxygen Layers," 2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, Singapore, 2020, pp. 1-4, doi: 10.1109/IPFA49335.2020.9260584 .

C15. Atsushi Shimbori, **Hiu Yung Wong** and Alex Q. Huang, "Fabrication and Analysis of a Novel High Voltage Heterojunction p-NiO/n-Ga2 O3 Diode," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020, pp. 218-221, doi: 10.1109/ISPSD46842.2020.9170054.

C16. Robert J Mears, Hideki Takeuchi, Yi-Ann Chen, Richard Burton, Shuyi Li, Robert J. Stephenson, Marek Hytha, Nyles W. Cody, K. Doran Weeks, Dmitri Choutov, Daniel Connelly and **Hiu-Yung Wong**, "Applications of Oxygen Inserted Silicon Devices in Power and RF: (invited)," 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Penang, Malaysia, 2020, pp. 1-4, doi: 10.1109/EDTM47692.2020.9117944. **(INVITED)**

C17. **Hiu Yung Wong**, Johan Saltin[+] and Yan Ka Chiu[+], "SRAM Radiation Effect Study using DTCO Approach," 16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics, San Jose, CA, Nov, 2019. **(INVITED)**

C18. **Johan Saltin**[+] and **Hiu Yung Wong,** "TCAD Simulation of FinFET and Nanosheet Radiation Hardness," 16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics, San Jose, CA, Nov, 2019. (Poster)

C19. **Johan Saltin**[+], Shiyang Tian, Fei Ding and **Hiu Yung Wong**, "Novel Doping Engineering Techniques for Gallium Oxide MOSFET to Achieve High Drive Current and Breakdown Voltage," IEEE 7th Workshop on Wide Bandgap Power Devices and Applications, Raleigh, NC, 2019, pp261-264.

C20. **Khoa Huynh**[+], Johan Saltin[+], Jin-Woo Han, Meyya Meyyappan and **Hiu Yung Wong**, "Study of Layout Dependent Radiation Hardness of FinFET SRAM using Full Domain 3D TCAD Simulation," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, San Jose, CA, 2019.

C21. **J. Saltin**[+], N. C. Dao, P. H. W. Leong, and **H. Y. Wong**, "Degradation of Sub-Threshold Slope in Ultra-Scaled MOSFETs due to Energy Filtering at Source Contact," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, San Jose, CA, 2019.

C22. **K. Huynh**[+], A. C. Tenkeu[+], K.P. Pun and **H. Y. Wong**, "TCAD-Spice Co-Simulation of Ferroelectric Capacitor as an Electrically Trimmable On-Chip Capacitor in Analog Circuit", IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, San Jose, CA, 2019.

C23. **Bankapalli Yogeswara Sarat**[+] and **Hiu Yung Wong**, "TCAD Augmented Machine Learning for Semiconductor Device Failure Troubleshooting and Reverse Engineering", IEEE 2019 International Conference on Simulation of Semiconductor Processes and Devices, Udine, Italy, 2019, pp. 21-24.

C24. Ravi Tiwari, Narendra Prihar, Karansingh Thakor, **Hiu-Yung Wong** and Souvik Mahapatra, "TCAD Framework to Estimate the NBTI Degradation in FinFET and GAA NSFET Under Mechanical Strain", IEEE 2019 International Conference on Simulation of Semiconductor Processes and Devices, Udine, Italy, 2019, pp. 9-12.

C25. **Hiu Yung Wong,** Nelson Braga, Jie Liu and R. V. Mickevicius, " Studies of Stress Effects on the Electrical Performance of AlGaN/GaN HEMTs through Ab-Initio Calculation and TCAD Simulation," 13th International Conference on Nitride Semiconductors 2019 (ICNS-13). (Poster)

C26. **H. Y. Wong,** F. Ding, N. Braga, R. V. Mickevicius, "Normally-off Dual-gate Ga_2O_3 Planar MOSFET and FinFET with High Current and Breakdown Voltage," International Symposium on Power Semiconductor Devices and ICs 2018, pp. 379-382. (Poster)

C27. **Hiu Yung Wong**, Munkang Choi, Ravi Tiwari and Souvik Mahapatra, "On the NBTI of Junction-less Nanowire and Novel Operation Scheme to Minimize NBTI Degradation in Analog Circuits", 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 172-175.

C28. N. Parihar, R. Tiwari, C. Ndiaye, M. Arabi, S. Mhira, **H. Wong**, S. Motzny, V. Moroz, V. Huard and S. Mahapatra, "Modeling of Process (Ge, N) Dependence and Mechanical Strain Impact on NBTI in RMG HKMG SiGe FDSOI p-MOSFETs and p-FinFETs", 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 167-171.

C29. P. Pfäfflia, **H.Y. Wong**, X. Xu, L. Silvestria, X.W. Lin, T. Yang, R. Tiwari, S. Mahapatra, S. Motzny, V. Moroz and Terry Ma, "TCAD Modeling for Reliability," in 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis **(INVITED)**

C30. Pooya Jannaty, **Hiu-Yung Wong**, Ricardo Borges, Lee Smith, "A physics-based industry-proven TCAD simulator for superconducting electronics," Applied Superconductivity Conference 2018. (POSTER)

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C44. **H. Y. Wong,** H. Takeuchi, A. Padilla, T.-J. King, M. Ameen, and A. Agarwal, "Pulsed excimer laser annealing for meeting near-term front end processes gate-stack challenges," presented at the 207th Meeting of the Electrochemical Society, Symposium K1 (Quebec City, Canada), May 2005.

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C46. H. Takeuchi, **H. Y. Wong**, D. Ha, and T.-J. King, "Impact of oxygen vacancies on high-k gate dielectric engineering," International Electron Devices Meeting Technical Digest, pp. 829-832, 2004.

C47. **H. Y. Wong**, K. Shin, and M. Chan, "The Gate Misalignment Effects of the Sub-threshold Characteristics of sub-100nm DG-MOSFETs", 2002 IEEE Hong Kong Electron Devices Meeting Proceedings, pp. 91-94, June 22, 2002, Hong Kong

C48. Neil N. H. Ching, **Hiu Yung Wong**, Wen J. Li, and Philip H. W. Leong, "A laser-micromachined vibrational to electrical power transducer for wireless sensing systems", 11th International Conference on Solid-State Sensors and Actuators, (Transducers '01 / Eurosensors XV), Munich, Germany, June 2001.

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C50. Wen J. Li, Philip H. W. Leong, Terry C. H. Hong, **Hiu Yung Wong**, and Gordon M. H. Chan, "Infrared Signal Transmission by a Laser-micromachined vibration-induced power generator", Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, August 8-11, pp. 236-239, 2000

C51. **H. Y. Wong**, W. S. Yuen, K. H. Lee and P. H. W. Leong, "A Runtime Reconfigurable Implementation of the GSAT Algorithm", the Proceedings of the Ninth International Workshop on Field Programmable Logic and Applications (FPL'99) Glasgow, UK, pp. 526-531, 1999

Invited Conference Workshops and Tutorials:

W1. **Hiu Yung Wong,** Workshop 1: Combination of TCAD and Machine Learning**,** SISPAD 2020

W2. **Hiu Yung Wong,** (Ultra) Wide Bandgap Material Process and Device TCAD Simulation Methodologies, WiPDA-Asia, 2020

Invited Presentations (+: Supervised Students)

I1. **Hiu Yung Wong**, Nelson Braga, and R. V. Mickevicius, TCAD modeling of hydrogen-terminated diamond FET for RF Applications, Mat Science 2020, San Francisco, CA, November 5-7, 2020.

I2. **Hiu Yung Wong**, "TCAD to SPICE:MST RF Simulation as an Example", Atomera, Inc., Saratoga, CA, Sept. 2020.

I3. **Hiu Yung Wong**, "TCAD Seminar: Using Machine Learning in TCAD", Synopsys, Inc., Mountain View, CA, Aug. 2020.

I4. **Hiu Yung Wong**, Modeling, Calibration and Simulation of Ga2O3 Vertical Diode and FinFET in TCAD, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2020.

I5. **Hiu Yung Wong**, "TCAD Augmented Machine Learning for Semiconductor Device Failure Troubleshooting and Reverse Engineering", Silvaco, Inc., Santa Clara, CA, Oct 2019.

I6. **Hiu Yung Wong** and Johan Saltin^{+}, TCAD Simulation of Novel Gallium Oxide Power Device with High On/Off Ratio, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2019.

I7. Rake-Gate AlGaN/GaN normally off HEMTs, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2018.

I8. **Hiu Yung Wong**, "Selected TCAD Topics on More Moore and More than Moore", Seminar Talk in Department of Electronic Engineering, Chinese University of Hong Kong, Hong Kong, 2017.

I9. Low RC-constant Perforated-Channel HFET, Workshop on Compound Semiconductor Materials and Devices WOCSEMMAD, 2014,

I10. **Hiu Yung Wong,** "Elimination of Poly-Si Gate Depletion for Sub-65nm CMOS Technologies by Excimer Laser Annealing", West Coast Junction Technology Group Meeting, Sunnyvale, CA, 2005.

I11. **Hiu Yung Wong**, Laser Annealing Technology, AMD, Sunnyvale, CA, 2005.

Other Technical Publications

- Subrat Mishra, Narendra Parihar, Rakesh Rao, and Souvik Mahapatra, **Hiu Yung Wong**, Steve Motzny, and Victor Moroz, "NBTI Modeling in Sentaurus Device", Synopsys TCAD Newsletter December 2016.
- TCAD Application Note "Device Monte Carlo Simulation Methodology of Two-dimensional FinFET Slices", 2012
- TCAD Application Note "Simulation of Normally Off GaN MISFET with Piezo Neutralization Technique", 2011
- TCAD Application Note "Simulation of Normally Off AlGaN/GaN HFETwith p-Type GaN Gate and AlGaN Buffer", 2011
- SRC Report on tunable work function gate technology options (2-Aug-2004). Publication: P009712 (with K. Shin).
- 0.35um CMOS Process on Six-inch Wafers Baseline Report IV, A. Horvath, S. Parsa and **H. Y. Wong**, Memorandum No. UCB/ERL M05/15, Electronics Research Laboratory, College of Engineering, UC Berkeley
- **H Wong**, N Braga, S Tian, R Borges, "Simulations Enhance The Development Of Power Devices", compound semiconductor, 2011

Teaching/Mentoring/Training Experience

- **Lecturer**

EE124. Electronic Design II, San Jose State University, (57 students), Spring 2021
EE224. High Speed CMOS Circuits, San Jose State University, (26 students), Spring 2021
EE124. Electronic Design II, San Jose State University, (66 students), Fall 2020
EE222. Advanced Integrated Device, San Jose State University, (16 students), Spring 2020
EE124. Electronic Design II, San Jose State University, (57 students), Spring 2020
EE225. Introduction to Quantum Computing, San Jose State University, (12 students), Spring 2020
EE124. Electronic Design II, San Jose State University, (56 students), Fall 2019

EE224. High Speed CMOS Circuits, San Jose State University, (18 students), Fall 2019
EE124. Electronic Design II, San Jose State University, (58 students), Spring 2019
EE222. Semiconductor Devices II, San Jose State University, (13 students), Spring 2019
EE124. Electronic Design II, San Jose State University, (68 students), Fall 2018
EE224. High Speed CMOS Circuits, San Jose State University, (31 students), Fall 2018

- **Teaching Assistant experience (from Devices to Digital/Analog Circuits to Computer Architectures):**
  Microelectronic Devices and Circuits (EE 105), EECS, UC Berkeley, Fall 2005, ***evaluation: 4.4/5***
  Analog Integrated Circuits (EE 140), EECS, UC Berkeley, Fall 2001, ***evaluation: 4.4/5***
  Computer System Architectures (CEG 3420), CSE, CUHK, Spring 2001
  Digital Circuits (CEG 3470), CSE, CUHK, Fall 2000
  Computer System Architectures (CEG 3420), CSE, CUHK, Spring 2000, ***Best TA Award***
  Digital Circuits (CEG 3470), CSE, CUHK, Fall 1999, ***Best TA Award***

- **10-year TCAD and device physics training experience to customers**